#13 Appeal Briefs. Y. Edwards 11/5/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Rana P. Singh
Serial No.: 10/045913
Filed: January 9 , 2002
For: SEMICONDUCTOR DEVICE STRUCTURE AND METHOD FOR FORMING

October 20, 2003

Art Unit: 2811
Examiner: Samuel A. Gebremariam
Docket No.: SC11448TP-P01

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APPELLANTS' BRIEF ON APPEAL

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BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Authorization to charge Appellants' deposit account for fees associated with filing this Appeal Brief is provided in an accompanying Fee Transmittal paper.

REAL PARTY IN INTEREST

The present application is wholly assigned to MOTOROLA, INC., a Delaware corporation with its headquarters in Schaumburg, Illinois.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-10, 15-34, and 38-42 are the subject of this appeal. Claims 1-10, 15-34, and 38-42 were presented to the USPTO for the first time on January 9, 2002, the filing date of the present application. [Note: The present application is a continuation in part of U.S. patent application (09/997,145).] In a first Office Action, the Examiner issued a restriction requirement between device claims 11-14 and 35-37 and process claims 1-10, 15-34, and 38-42. Appellants responded by electing process claims 1-10, 15-34, and 38-42, with traverse. In a second Office Action, the Examiner rejected claims 1-3, 5, 8-10, 15, 19, 23-27, and 29 under 35 USC 102 (e) as being anticipated by Shiozawa et al. (US Patent 6,245,641), rejected claims 4, 6, 16, 17, 18, 22, 28, 32, 40, and 42 under 35 USC 103(a) as being unpatentable over the same reference, and rejected claims 7, 18, 20, and 21 under 35 USC 103(a) as being unpatentable over Shiozawa in view of Lee (US Patent 5,994,201), and rejected claims 38-42 under 35 USC 103(a) as being unpatentable over Shiozawa in view of Koike (US Patent 5,578,518). Appellants responded to the rejection with arguments and cancelled non-elected claims 11-14 and 35-37. In this response, Appellants also amended claims 1, 5, 15, 19, 20, 26, and 29. The Examiner finally rejected the claims on the same grounds as originally rejected. Appellants responded in an after final response with arguments. At this point, claims 1-10, 15-34, and 38-42 were still pending. The Examiner did not find Appellants'

arguments persuasive. Thus, Appellants submitted a Notice of Appeal on July 22, 2003. This Appeal Brief is being submitted in support of the Notice of Appeal.

STATUS OF AMENDMENTS

The claims being appealed are claims 2-4, 6-10, 16-18, 21-25, 27-28, 30-34, and 38-42 as originally filed, and claims 1, 5, 15, 19, 20, 26, and 29 as amended in Appellants' reply submitted February 5, 2003.

SUMMARY OF THE INVENTION

Appellants' invention relates generally to semiconductor device structures, and more specifically to trench isolation structures. System on a chip solutions require the ability to fabricate different semiconductor device structures into a same chip. However, different semiconductor device structures may have different isolation requirements. For example, system on a chip solutions may require both a non-volatile memory (NVM) device and logic to be within the same chip. Trenches within an NVM device, though, generally require wider trenches with a thicker oxide lining and greater trench corner rounding as compared to trenches outside the NVM device. Therefore, different regions within a chip may require different trench widths. Embodiments of the present invention allow for sufficient liner thicknesses and sufficient corner rounding for both narrower and wider width trenches while preventing the formation of voids within the narrower width trenches.

FIG. 1 illustrates one embodiment of a semiconductor device structure 10 having a narrower width trench 18 and a wider width trench 20 within a substrate 12, a stress relief layer 14, and a barrier layer 16. FIG. 2 illustrates semiconductor device structure 10 after formation of liner layers 22 and 24 within trenches 18 and 20. In one embodiment, these liners are formed by thermally growing oxide within the trenches (see page 5, lines 16-18, of the present application). The grown oxide within trenches 18

and 20 therefore allow for sufficient degrees of corner rounding (illustrated in FIG. 2 as corners 21 and 23) in different regions of an integrated circuit (see page 7, lines 1-6, of the present application). In FIG. 3, a masking layer 26 is formed overlying wider width trench 20 (see page 7, lines 15-18, of the present application), and in FIG. 4, an etch is performed to remove at least a portion of liner layer 22 within narrower width trench 18 (see page 7, lines 18-22, of the present application). In one embodiment, all of liner layer 22 may be removed. FIG. 5 illustrates semiconductor device structure 10 after removing masking layer 26 and subsequently forming a trench fill layer 30.

In an alternate embodiment illustrated in FIG. 6, after completing the structure illustrated in FIG. 2 (that is, after formation of liner layers 22 and 24), at least a portion of both liner layers 22 and 24 is removed (see page 10, lines 3-15, of the present application). In one embodiment, all of liner layers 22 and 24 may be removed. Therefore, in this embodiment, a masking layer such as masking layer 26 of FIGs. 3 and 4 is not needed. FIG. 7 illustrates the semiconductor device structure of the embodiment of FIG. 6 after subsequently forming a trench fill layer 30.

Therefore, note that in either embodiment (where at least a portion of liner 22 is removed with the use of masking layer 26 or where at least a portion of both liners 22 and 24 is removed without requiring the use of masking layer 26), isolation trenches of different widths may be formed in different regions of an integrated circuit while still allowing for sufficient liner thicknesses and sufficient corner rounding, due, for example, to the thermally grown oxide liners 22 and 24 (see page 8, line 25, to page 9, line 8, and see page 11, line 15, to page 12, line 8, of the present application).

ISSUES

1) Are claims 1-3, 5, 8-10, 15, 19, 23-27, and 29 anticipated by Shiozawa et al. (US 6,245,641) under 35 U.S.C. 102(e)?

2) Are claims 4, 6, 16, 17, 18, 22, 28, 30-34, 40, and 42 unpatentable over Shiozawa et al. (US 6,245,641) under 35 U.S.C. 103(a)?
3) Are claims 7, 18, 20, and 21 unpatentable over Shiozawa et al. (US 6,245,641) in view of Lee (US Patent 5,994,201) under 35 U.S.C. 103(a)?
4) Are claims 38-42 unpatentable over Shiozawa et al. (US 6,245,641) in view of Koike (US Patent 5,578,518) under 35 U.S.C. 103(a)?

GROUPING OF CLAIMS

Group A → Claims 1-10 and 15-28
Group B → Claims 29-34 and 38-42

The requested division is on the basis that the claims of Group A are directed to a method for forming a semiconductor device structure including forming a first trench and a second trench in a semiconductor layer, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching at least a portion of the first insulator liner. The claims of Group A stand or fall together. The claims of Group B are directed to a method for forming a semiconductor device structure including forming a first trench and a second trench in a semiconductor layer, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching a portion of the first insulator liner and a portion of the second insulator liner. The claims of Group B stand or fall together.

ARGUMENTS

Arguments Common to Groups A and B

Rejections under 35 U.S.C. 102(e) →

The Examiner uses Shiozawa in the rejections of claims 1, 2, 5, 8-10, 15, 19, 23-27 of Group A and claim 29 of Group B under 35 U.S.C. 102(e). In regards to the rejections using Shiozawa under 35 U.S.C. 102(e), Appellants respectfully submit that claims 1,2, 5, 8-10, 15, 19, 23-27, and 29 are not anticipated by the cited prior art. A reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984).

More specifically, with respect to independent claims 1, 15, 26, and 29, Appellants submit that Shiozawa does not or suggest each and every element recited in claims 1, 15, 26, and 29. That is, each of claims 1, 15, 26, and 29 include forming a first trench and a second trench, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching at least a portion of the first insulator liner. In the Office Action mailed April 22, 2003, the Examiner states that the first insulator liner is taught by layer 5b of Shiozawa and that the second insulator liner is taught by layers 5a and 8 of Shiozawa. However, Appellants respectfully submit that the Examiner has mischaracterized the claims and the prior art reference. Firstly, layers 5a and 8 together should not be considered a second insulator liner because they are formed at different times using different processes. Secondly, although portions 5a and 5b of Shiozawa are thermal oxides, silicon oxide film 8 (as stated in col. 10, lines 5-10, of Shiozawa) is deposited by chemical vapor deposition (CVD) and not grown. Therefore, layers 5a and 8 together of Shiozawa cannot be considered to be the *grown* second insulator liner.

In the Advisory Action mailed July 16, 2003, the Examiner states that "growing an oxide layer is the same as depositing an oxide layer." However, Appellants respectfully submit that this is incorrect. Growing is not the same as depositing an oxide layer. For example, a grown oxide generally results in a higher quality oxide as compared to a deposited oxide. Also, a grown oxide may be better able to achieve other benefits such as corner rounding. Furthermore, it may not be possible to grow an oxide. For example, the high temperature required in growing the oxide may damage other portions of the wafer, or there may not be a suitable material on which to grow the oxide. Therefore, there are many situations in which one form of an oxide (grown or deposited) is preferable or required over the other. For the Board's reference, Appellants are also providing herein (as Exhibit A) an excerpt (pp. 109-110) from the book "*Silicon Processing for the VLSI Era*," by S. Wolf and R.N. Tauber which is intended to provide further support that growing and depositing layers is not the same. This excerpt divides the formation of thin films into two separate groups: 1) film growth by interaction of a vapor-deposited species with the substrate (this category includes thermal oxidation); and 2) film formation by deposition without causing changes to the substrate material (this category includes CVD). Therefore, it is incorrect for the Examiner to state that growing an oxide layer is the same as depositing an oxide layer.

Furthermore, as discussed in the previous paragraph, there are situations where one form of oxide may not be possible. For example, silicon oxide film 8 of Shiozawa cannot be grown since it must also be formed on the silicon nitride films 3a and 3d in order to prevent corner erosion of the nitride films 3a and 3b during the trench fill process (see col. 10, lines 5-10 and lines 45-65, of Shiozawa). That is, growing silicon oxide film 8 would destroy the functionality of Shiozawa because the silicon oxide would not grow on silicon nitride films 3a and 3d which is necessary in order for the structure of Shiozawa to operate properly. Therefore, for this additional reason, layers 5a and 8 of Shiozawa cannot be considered to be the grown second insulator liner.

Also, as stated above, each of claims 1, 15, 26, and 29 further claim *etching* a portion (or at least a portion) of the *grown* first insulator layer, and Shiozawa does not

teach or suggest this claim element. For example, Shiozawa does not teach or suggest the removal of oxide layer 5b (or the removal of oxide layer 5a). Unlike in claims 1, 15, 26, and 29, only the silicon oxide film 8 of the oxide layers of Shiozawa is ever removed (see Fig. 7 of Shiozawa). That is, Shiozawa does not teach or even suggest the etching of a *grown* insulator liner within the trenches.

In the Advisory Action mailed July 16, 2003, the Examiner also states that "unless the claims explicitly state that the oxide layers are thermally grown, the process is not patenably [sic] distinct from any other deposition process." However, note that claims 1, 15, 26, and 29 are directed to growing insulating layers, and are not limited to growing oxides. Some of the dependent claims, such as claims 5 and 19 do specifically recite growing an oxide, but Appellants submit that one of ordinary skill in the art knows that growing an oxide layer results in a thermally grown oxide layer. That is, a grown oxide layer is the same as a thermally grown oxide layer; therefore, the claims which refer to growing oxides need not explicitly state that they are thermally grown.

For the above reasons, Shiozawa fails to teach or suggest forming a first trench and a second trench, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching at least a portion of the first insulator liner, as claimed in claims 1, 15, 26, and 29. For at least these reasons, independent claims 1, 14, 26, and 29 and dependent claims 2-10, 16-25, 27-28, and 20-34 are patentable over Shiozawa under 35 U. S.C. 102(e), and reversal is respectfully requested.

Rejections under 35 U.S.C. 103(a) →

In regards to the rejections under 35 U.S.C. 103(a), Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, which is the burden of the USPTO when rejecting claims under 35 U.S.C. 103(a). *In re Reuter*, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). The case of prima facie obviousness is not met because the references cited by the Examiner in support of the rejection do not teach

or suggest all of the claim limitations recited in claims 3, 4, 6, 7, 16, 17, 18, 20-22, 28, 30-34, and 38-42. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970); *In re Fine*, 5 USPQ2d 1596 (CAFC 1988).

More specifically, with respect to independent claim 38, Appellants submit that Shiozawa does not or suggest each and every element recited in claim 38. That is, claim 38, like claims 1, 15, 26, and 29, also includes forming a first trench and a second trench, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching at least a portion of the first insulator liner. In the Office Action mailed April 22, 2003, the Examiner states that Shiozawa teaches these elements of claim 38. However, Appellants respectfully disagree. (Note that the Examiner uses a second reference, Koike, to provide a teaching of other elements in claim 38.)

As discussed above in reference to claims 1, 15, 26, and 29, Shiozawa does not teach or suggest growing the second insulator liner in a second trench, as claimed. Firstly, layers 5a and 8 together should not be considered the second insulator liner because they are formed at different times using different processes. Secondly, silicon oxide film 8 is deposited and not grown. Furthermore, as discussed above, the silicon oxide film 8 of Shiozawa cannot be grown because this would destroy the functionality of Shiozawa. In addition to these reasons, Shiozawa also does not teach or suggest etching the grown insulator liner. For example, Shiozawa does not teach or suggest etching layer 5b (or layer 5a). That is, unlike in claim 38, only the silicon oxide film 8 of the oxide layers of Shiozawa is ever removed (see, Fig. 7 of Shiozawa). Furthermore, these elements are also not taught or suggested by Koike, which the Examiner cited as teaching the radius of curvature claimed in claim 38.

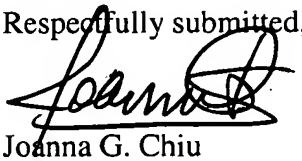
A prima facie case of obviousness therefore has not been established because Shiozawa and Koike (alone or in combination) do not teach or suggest each and every element of claim 38. Thus, for at least these reasons, Appellants submit that independent claim 38 and dependent claims 39-42 are patentable over Shiozawa in view of Koike under 35 U.S.C. 103(a), and reversal is respectfully requested. Also, claims 3,

4, 6, 7, 16, 17, 18, 20-22, 28, and 30-34 depend directly or indirectly from claims 1, 15, 26, and 29 and are therefore also allowable over Shiozawa in view of Koike under 35 U.S.C. 103(a) for at least those reasons provided above with respect to claims 1, 15, 26, and 29. Reversal as to these dependent claims is therefore also respectfully requested.

Additional Arguments for Group B

The Examiner uses Shiozawa in the rejections of claims 29-34 and 38-42 of Group B. With respect to claim 29, Shiozawa does not teach or suggest each and every element of claim 29, as described above. Similarly, the Examiner has failed to make a prima facie case of obviousness with respect to claim 38, as described above. However, in addition to forming a first trench and a second trench, growing a first insulator liner in the first trench and a second insulator liner in the second trench, and etching at least a portion of the first insulator liner, each of claims 29 and 38 also claim etching at least a portion of the second insulator liner. As described above, none of the cited prior art teach or suggest each and every one of these elements. For example, as described above, in the Office Action mailed April 22, 2003, the Examiner states that the first insulator liner is taught by layer 5b of Shiozawa and that the second insulator liner is taught by layers 5a and 8 of Shiozawa. However, Shiozawa does not teach or suggest etching a portion of the *grown* first insulator liner *and* a portion of the *grown* second insulator liner. For example, Shiozawa does not teach or suggest etching either layers 5a or 5b. Therefore, for these additional reasons, Appellants respectfully submit that the claims of Group B are allowable. Reversal is respectfully requested.

Respectfully submitted,



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APPENDIX

1. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench;

etching at least a portion of the first insulator liner while the mask is over the second trench;

removing the mask; and

depositing an insulating layer in the first trench and the second trench.

2. The method of claim 1, wherein the first width is less than the second width.

3. The method of claim 1, wherein the step of etching comprises completely removing the first insulator liner.

4. The method of claim 1, wherein the step of etching results in leaving at least one hundred Angstroms of the first insulator liner.

5. The method of claim 1, wherein the step of growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

6. The method of claim 1, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

7. The method of claim 1, wherein the step of etching comprises applying a dry etch chemistry to the semiconductor device structure.

8. The method of claim 1, wherein the insulator layer comprises high density plasma oxide fill.

9. The method of claim 1, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

10. The method of claim 1, further comprising forming a pad nitride and pad oxide over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer.

15. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer, the first width being less than the second width;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench; and

etching at least a portion of the first insulator liner while the mask is over the second trench.

16. The method of claim 15, wherein the step of etching comprises a wet etch.

17. The method of claim 16, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

18. The method of claim 15, wherein the etching comprises a dry etch.

19. The method of claim 15, wherein the step of growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

20. The method of claim 15, wherein:

the semiconductor layer has a top surface;

the second trench has a corner where the trench adjoins the top surface of the semiconductor layer; and

the step of growing the first insulator liner and the second insulator liner comprises rounding of the corner of the second trench.

21. The method of claim 20, wherein the corner is semiconductor.

22. The method of claim 15, wherein the step of etching comprises leaving at least 100 Angstroms of the first insulating liner.

23. The method of claim 15, wherein the step of etching comprises removing the first insulating liner.

24. The method of claim 15, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

25. The method of claim 24, wherein the barrier layer comprises nitride and the stress relief layer comprises oxide.

26. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width greater than the first width in the second semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner; and

depositing an insulating layer in the first trench.

27. The method of claim 26 further comprising

forming a mask over the second trench prior to the step of etching; and

removing the mask prior to the step of depositing.

28. The method of claim 26, wherein the step of etching further comprises etching a portion of the second insulator liner and leaves at least 50 Angstroms of the first insulator liner and 50 Angstroms of the second liner.

29. A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width in the second semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench.

30. The method of claim 29, wherein the step of etching comprises a wet etch.

31. The method of claim 30, wherein the wet etch uses hydrofluoric acid.

32. The method of claim 29, wherein the first insulator and the second insulator liner comprises thermal oxide.

33. The method of claim 29, wherein the step of depositing comprises filling the first trench and second trench.

34. The method of claim 33, wherein the insulating layer comprises high density plasma oxide.

38. A method for forming a semiconductor device structure in a semiconductor layer having a top surface, comprising:

forming a first trench of a first width in the semiconductor layer and having a first corner at the surface of the semiconductor layer;

forming a second trench of a second width greater than the first trench in the second semiconductor layer and having a second corner at the surface of the semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench that fills the first and second trenches, wherein the insulating layer is free of voids.

39. The method of claim 38, wherein the first insulator liner and the second insulator liner are thermal oxide.

40. The method of claim 38, wherein the step of etching leaves the first insulator liner and the second insulator liner at a thickness sufficiently small to allow for completely filling the first trench with the insulating layer without voids in the insulating layer.

41. The method of claim 40, wherein the insulating layer comprises high density plasma oxide.

42. The method of claim 38, wherein the step of etching is further characterized as leaving at least 50 Angstroms of the first insulator liner and the second insulator liner.